What is claimed is:

[Claim 1] A method for predicting semiconductor yield, comprising the steps of:

(a) calculating yield for at least one sampling region in a set of sampling regions on a semiconductor wafer; and,
(b) predicting yield of a semiconductor wafer based upon at least said calculated yield of said at least one sampling region.

[Claim 2] A method as in claim 1, further comprising, the step of:

partitioning a semiconductor wafer into a set of sampling regions, prior to step (a), said set comprising at least two sampling regions.

[Claim 3] A method as in claim 1, wherein at least one sampling region comprises a shape of at least one of a quadrant, a slice, and a ring.

[Claim 4] A method as in claim 1, wherein said at least one sampling region on said semiconductor wafer comprises at least one die and step (a) further comprises:

(a1) testing said at least one die in said at least one sampling region; and,
(a2) determining said calculated yield of said at least one sampling region based upon results of said step (a1).

[Claim 5] A method as in claim 1, wherein said predicted yield of said semiconductor wafer is based further upon calculated yield of a combination of sampling regions.

[Claim 6] A method as in claim 1, further comprising, the step of:

(c) calculating yield for a second sampling region in said set of sampling regions on said semiconductor wafer;
wherein said second sampling region neighbors said first sampling region.

[Claim 7] A method as in claim 6, further comprising, the steps of:

(d) comparing said calculated yield of said first sampling region with said calculated yield of said second sampling region; and,
(e) subsuming said second sampling region into said first sampling region whenever said calculated yield of said first sampling region is substantially similar to said calculated yield of said second sampling region.

[Claim 8] A method as in claim 7, wherein step (b) further comprises, the step of:

(b1) predicting yield of said semiconductor wafer based upon said first sampling region with said subsumed second sampling region whenever said predicted yield of said first sampling region is substantially similar to said predicted yield of said second sampling region.

[Claim 9] A method as in claim 1, further comprising, the steps of:

(c) comparing said calculated yield of said at least one sampling region with a target yield for said sampling region; and
(d) discontinuing further testing of said at least one sampling region, whenever said calculated yield does not substantially equal said target yield.

[Claim 10] A method as in claim 1, further comprising, the step of:

(c) repeating steps (a) - (b) for a predetermined number of semiconductor wafers.

[Claim 11] A method as in claim 10, further comprising, the step of:

(d) predicting total yield for said predetermined number of semiconductor wafers.

[Claim 12] A method as in claim 11, further comprising, the step of:

(e) comparing said predicted total yield for said predetermined number of semiconductor wafers with a target yield for said predetermined number of semiconductor wafers.

[Claim 13] A method as in claim 12, further comprising, the step of:

(f) initiating a semiconductor wafer fabrication run whenever said predicted total yield does not satisfy said target yield for said predetermined number of semiconductor wafers.

[Claim 14] A method as in claim 12, further comprising, the step of:

(f) altering at least one semiconductor fabrication process condition whenever said predicted total yield for said predetermined number of semiconductor wafers does not satisfy said target yield for said predetermined number of semiconductor wafers.

[Claim 15] A method for calculating yield of a semiconductor wafer, comprising the steps of:

(a) determining a boundary for a sampling region on a semiconductor wafer, said first sampling region comprising at least one die; and,
(b) calculating yield of a representative sampling of said die in said boundary of said sampling region.

[Claim 16] A method as in claim 15, further comprising, the steps of:

(c) determining a latest boundary for said sampling region on said semiconductor wafer, said latest boundary comprising at least one of at least

one more die and at least one less die of said sampling region of a previous boundary; and,
(d) calculating yield of a representative sampling of said die in said latest boundary of said sampling region.

[Claim 17] A method as in claim 16, further comprising, the step of:

(e) repeating steps (c) – (d) until said calculated yield for said sampling region with said latest boundary satisfies a target yield for at least one of said sampling region and said semiconductor wafer.

[Claim 18] A method as in claim 17, further comprising, the step of:

(f) repeating steps (a) – (e) for a predetermined number of sampling regions on said semiconductor wafer.

[Claim 19] A method as in claim 18, further comprising, the step of:

(g) identifying a combination of sampling areas with a total predicted yield that satisfies said target yield for said semiconductor wafer.

[Claim 20] A method as in claim 19, further comprising, the step of:

(h) discontinuing further testing of sampling regions that have not been identified in said combination.

[Claim 21] A method as in claim 17, further comprising, the step of:

(f) predicting yield of said semiconductor wafer based upon said predicted yield of said sampling region.

[Claim 22] A method as in claim 18, further comprising, the step of:

(g) predicting yield of said semiconductor wafer based upon a combination of a predetermined number of sampling regions.

[Claim 23] A method as in claim 18, further comprising, the step of:

(g) repeating steps (a) - (f) for a predetermined number of semiconductor wafers.

[Claim 24] A method as in claim 23, further comprising, the step of:

(h) predicting total yield for said predetermined number of semiconductor wafers.

[Claim 25] A method as in claim 24, further comprising, the step of:

(i) comparing said total yield for said predetermined number of semiconductor wafers with a target yield for said predetermined number of semiconductor wafers.

[Claim 26] A method as in claim 25, further comprising, the step of:

(j) initiating a new semiconductor fabrication run whenever said total yield for said predetermined number of semiconductor wafers does not substantially equal said target yield for said predetermined number of semiconductor wafers.

[Claim 27] A method as in claim 25, further comprising, the step of:

(j) altering at least one semiconductor fabrication process condition whenever said total yield for said predetermined number of semiconductor wafers does not substantially equal said target yield for said predetermined number of semiconductor wafers.

[Claim 28] A computer software program adapted to execute a method comprising the steps of: (a) calculating yield for at least one sampling region in a set of sampling regions on a semiconductor wafer; and, (b) predicting yield of said semiconductor wafer based upon at least said calculated yield of said at least one sampling region.

[Claim 29] A computer software program adapted to execute a method comprising the steps of:

(a) determining a boundary for a sampling region on a semiconductor wafer, said first sampling region comprising at least one die;
(b) calculating yield of a representative sampling of said die in said boundary of said sampling region;
(c) determining a latest boundary for said sampling region on said semiconductor wafer, said latest boundary comprising at least one of at least one more die and at least one less die of said sampling region of a previous boundary;
(d) calculating yield of a representative sampling of said die in said latest boundary of said sampling region; and,
(e) repeating steps (c) – (d) until said calculated yield for said sampling region with said latest boundary satisfies a target yield for at least one of said sampling region and said semiconductor wafer.